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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
00100.99.0068

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on March 16, 2009

Signature Robert Holland

Typed or printed name Robert Holland

Application Number	Filed
09/398,913	September 14, 1999

First Named Inventor
Ilya Klebanov

Art Unit	Examiner
2421	Oschta I. Montoya

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☑ attorney or agent of record.
Registration number 62,264

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

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March 16, 2009
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ilya Klebanov	Examiner:	Oschta I. Montoya
Appl. No.:	09/398,913	Art Group:	2421
Filing Date:	September 14, 1999	Our File No.:	00100.99.0068
Conf. No.:	1646		
Title:	**METHOD AND APPARATUS FOR RECEIVING DIGITAL VIDEO SIGNALS**		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REMARKS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Applicants respectfully submit that the Examiner's rejections include clear errors because one or more claim limitations are not met by the cited reference and the reference does not teach what the Examiner alleges.

Claims 14–16 and 24–25 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Cheney (U.S. Pat. No. 6,519,283) in view of So (U.S. Pat. No. 5,909,559). With regard to claim 14, Cheney fails to show, teach, or suggest, inter alia, generating a secondary set of memory control signals from the compressed transport stream's control signals. As best understood by Applicants, Cheney discloses an integrated digital video system configured to implement picture-in-picture merging of video signals from two or more video sources. The picture-in-picture signal is produced for display by a television system lacking picture-in-picture capability. In one implementation, a decompressed digital video signal is downscaled and merged with an uncompressed video signal to produce the multi-screen display.

The Examiner states the following:

> The claimed "generating a secondary set of memory control signals from the compressed transport stream's control signals" is met by the video decode system of Figure 6 and is

> further described in col. 9, line 9 – col. 13, line 36, where an MPEG input source signal is received at the memory control unit 652 and numerous control signals, which include at least the claimed "secondary set of memory control signals", are generated from the compressed transport stream or MPEG input source and memory control unit. (See p. 5 of Final Office Action dated November 14, 2008.)

However, as best understood by Applicants, the cited portions merely disclose that an internal processor oversees the video decode process and receives a signal from a host system whenever the host desires to switch the video display between normal video display and scaled video display. In response to host format changes, control signals are sent from the internal processor to a Huffman decoder, an Inverse Quantizer, a Motion Compensation, upsample logic, a display fetch unit, and display mode switch logic within video display. The control signals direct the video decode system to switch the display output between normal video mode and scaled video mode. As such, the control signals of Cheney merely control the display mode and are not memory control signals as required by the claim. Since the reference does not teach what is alleged, the Examiner has committed clear error that requires withdrawal of the rejection.

In addition, as noted above, the internal processor provides control signals in response to the host system when it desires to switch the video display between the normal video display and the scaled video display. As shown in FIG. 6, the internal processor 670 receives the host controlled format change directly from the host system and not from the MPEG input source. Therefore, the control signals disclosed in Cheney are not generated from the compressed transport stream's control signals as required by the claim. Since the reference does not teach what is alleged, the Examiner has committed clear error that requires withdrawal of the rejection.

Claim 25 is allowable for at least similar reasons as claim 14. Claims 15, 16, and 24 each ultimately depend on claim 14 and are allowable for at least similar reasons. Claims 15, 16, and 24 are also believed to be allowable for having novel and non-obvious subject matter.

Claims 18–20 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Schindler (U.S. Pat. No. 5,900,867) in view of So (U.S. Pat. No. 5,909,559). With regard to claim 18, the Examiner admits that Schindler fails disclose the video graphics adapter is operative to store at least a portion of compressed transport stream data signals to be at first in frame buffer memory controlled by a secondary set of memory control signals derived from the compressed transport streams control signals.

The Examiner cites col. 17, ll. 1–15 and col. 130, ll. 15 to col. 131, l. 30 and states the following:

> The video graphics adapter stores a portion of the compressed transport stream data signals in the frame buffer memory controlled by a secondary set of memory control signals derived from the compressed transport stream control signals and stores uncompressed data in the frame buffer memory in a different mode of operation. (See p. 11 of Final Office Action dated November 14, 2008.)

However, the cited portions merely disclose that legacy architecture and IEEE 1394 peripherals can require the PCI bus to carry video data. Where an IEEE 1394 camera is used for image/video capturing and the output of the camera is to be stored in the PC system, the VSP can first perform image/video data compression to prevent undue PCI bus congestion then bus-master the data across the PCI bus to host memory further relieving the host of the I/O chore. Conversely in a video/image playback function, the VSP can bus-master compressed MPEG/JPEG data from the host memory across the PCI bus to avoid congestion of the PCI bus. The VSP can then decompress the MPEG/JPEG data and pass the video/image data via a zoom video private bus directly to the frame buffer of the graphics/video adapter without congesting the PCI bus unduly.

One embodiment of the system 100 includes an enclosure 104 with a printed wiring board and one or more add-in cards holding components chosen, configured and combined for advantageous desk top computer or portable (e.g. notebook) application. A host CPU 106 with

multimedia extensions MMX is coupled to an embedded L2 cache 114 and additionally coupled to a DRAM main memory 110 via an improved north bridge chip 108. A main PCI bus 124 interconnects MPU 106 via north bridge 108 with a south bridge 134, and an improved USP smart hub 136.

The north bridge 108 has a bus bridge circuit and a DRAM memory controller (MCU). A PCI Bus bridge acts as a bus master when there is a host 106 initiated transfer between the CPU and bus 124, and as a target for transfers initiated from an agent on bus 124. The MCU in bridge 108 supplies DRAM addresses and DRAM control signals to main memory 110 and further interfaces with an embedded L2/L3 cache DRAM 112.

Applicants can find no mention of the video graphics adapter operative to store at least a portion of compressed transport stream data signals to be at first in frame buffer memory controlled by a secondary set of memory control signals derived from the compressed transport streams control signals in the cited portions of So. Since the reference does not teach what is alleged, the Examiner has committed clear error that requires withdrawal of the rejection. Claims 19 and 20 each ultimately depend of claim 18 and are allowable for at least similar reasons. Claims 19 and 20 are also believed to have novel and non-obvious subject matter.

Claim 21 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Schindler (U.S. Pat. No. 5,900,867) in view of Malladi (U.S. Pat. No. 5,912,676) and in further view of Datari (U.S. Pat. No. 6,418,169). The Examiner cites col. 11, l. 34 to col. 12, l. 3 of Schindler and states the following:

> The claimed first mode of operation comprising storing pixel information in a frame buffer of a video adapter, wherein one line of frame buffer memory is representative of one line of a video image to be displayed is met in part by receiving an uncompressed signal from a cable video source through connector 524 (Fig. 5), as described above, where the video signal may be buffered in VRAM 518 for output to a monitor (see col. 11, line 34 - col. 12, line 3). [See p. 13 of Final Office Action dated November 14, 2008.]

> The claimed second mode of operation comprising storing compressed transport stream data in the frame buffer, wherein one line of frame buffer memory is representative of onc transport stream packet is met in part by the Schindler et al reference, which also discloses receiving an MPEG transport stream from a digital video source Fig 4, as described above, wherc the compressed MPEG transport stream is sent to the PC1 bus 312, where the video graphics adapter card receives the MPEG stream through controller 510 (Fig. 5, col. 11, lines 34–37), and the MPEG data is routed to MPEG-2 decoder 512 with associated random access memory (DRAM 514), which is used as buffer in assisting with the decoding (see col. 11, lines 37–47). [See p. 14 of Final Office Action dated November 14, 2008.]

However, these portions merely disclose that a controller 510 is coupled to the PCI bus to receive MPEG encoded video, and other normal personal computer display information such as graphics and text. If controller 510 detects MPEG data on PCI bus 312, it routes it to a decoder 512 with associated DRAM 514. DRAM 514 is used as a buffer to assist in the decoding, since large amounts of data are required at one time to decode MPEG data. The decoded video signal in YUV color encoding is provided back to controller 510 which then places the video information into VRAM 518. Accordingly, these portions disclose storing two different types of information in two different buffers (i.e., DRAM 514 and VRAM 518)—not the same frame buffer as required by the claim. Since the reference does not teach what is alleged, the Examiner has committed clear error that requires withdrawal of the rcjection.

In view of the preceding discussion, reconsideration and withdrawal of thc rejection of the claims is respectfully requested and a Notice of Allowance is respectfully requested.

Respectfully submitted,

Date: March 16, 2009

By: _____
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